REYAX
TECHNOLOGY CORPORATION, LTD

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RYW9000 Series

Hardware Design Guide

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APPLICABILITY TABLE

PRODUCTS
RYW94AP
RYW94EU
RYW94NF
RYW94LA
RYW94CN

1. PINS ALLOCATION

1.1 Pin-out

Pin	Signal	I/O	Function	Type	Comment
Power Supply					
2	VCC	-	3.3V Main Power Supply	Power	
24	VCC	-	3.3V Main Power Supply	Power	
39	VCC	-	3.3V Main Power Supply	Power	
41	VCC	-	3.3V Main Power Supply	Power	
52	VCC	-	3.3V Main Power Supply	Power	
4	GND	-	Ground		
9	GND	-	Ground		
15	GND	-	Ground		
18	GND	-	Ground		
21	GND	-	Ground		
26	GND	-	Ground		
27	GND	-	Ground		
29	GND	-	Ground		
34	GND	-	Ground		
35	GND	-	Ground		
37	GND	-	Ground		
40	GND	-	Ground		
43	GND	-	Ground		
50	GND	-	Ground		
USB Interface (Standard Version only)					
36	USB D-	I/O	USB differential Data (-)		
38	USB D+	I/O	USB differential Data (+)		
SIM Card Interface					
8	SIMVCC	I/O	External SIM signal – Power supply for the SIM	1.8V	
10	SIMIO	I/O	External SIM signal - Data I/O	1.8V	
12	SIMCLK	O	External SIM signal – Clock	1.8V	
14	SIMRST	O	External SIM signal – Reset	1.8V	

Pin	Signal	I/O	Function	Type	Comment
UART Interface (UART Version only)					
23	TXD	I	Serial data input (TXD) from DTE	1.8V	
25	CTS	O	Output for Clear to send signal (CTS) to DTE	1.8V	
28	RTS	I	Input for Request to send signal (RTS) from DTE. If flow control is not used, the RTS must be connected to GND.	1.8V	See note below
30	DCD	O	Output for Data Carrier Detect (DCD) to DTE	1.8V	
31	RXD	O	Serial data output to DTE	1.8V	
44	RING	O	Output for Ring Indication (RI) to DTE	1.8V	
46	DTR	I	Input for Data Terminal Ready (DTR) from DTE	1.8V	
48	DSR	O	Output for Data Set Ready (DSR) to DTE	1.8V	
Miscellaneous Functions					
6	VREG_MSME	O	The pin is always HI while RYW9000 is working	1.8V	
22	RESET	I	Active low functional reset input to the card	1.8V	
42	STATUS_LED	O	Status indicator LED, Open drain output.	1.8V	
Reserved					
1	Reserved	-			
3	Reserved	-			
5	Reserved	-			
7	Reserved	-			
11	Reserved	-			
13	Reserved	-			
16	Reserved	-			
17	Reserved	-			
19	Reserved	-			

Reserved					
20	Reserved				
32	Reserved	-			
33	Reserved	-			
45	Reserved	-			
47	Reserved	-			
49	Reserved	-			
51	Reserved	-			

Note: When the UART signals are used as the communication port between the host and the modem, the RTS must be connected to GND (on the module side) if flow control is not used.
If the UART port is not used, all UART signals can be left disconnected.

Note: Unless otherwise specified, RESERVED pins must be left unconnected (floating).

2. POWER SUPPLY

The power supply circuitry and board layout are a very important part in the complete product design and they strongly reflect on the overall performance of the product, so please read carefully the requirements and the guidelines that will follow for a proper design.

2.1. Power Supply Requirements

The external power supply must be connected to VBATT signal and must fulfil the following requirements:

Power Supply	Value
Nominal Supply Voltage	3.3V
Supply Voltage Range	3 ~ 5.5V
Max ripple on module input supply	30mV

Note: The Operating Voltage Range MUST never be exceeded; care must be taken when designing the power section of the application to avoid having an excessive voltage drop.
If the voltage drop exceeds the limits, it could cause the module to Power Off.
The overshoot voltage (regarding MAX Extended Operating Voltage) and drop in voltage (regarding MIN Extended Operating Voltage) MUST never be exceeded;
The “Extended Operating Voltage Range” can only be used with the complete assumption and application of the HW User guide suggestions.

2.2. Power Consumption

Table provides typical current consumption values of LE910Cx for the various available modes.

Mode		Average(Typ.)	Mode Description
Idle Mode (Standby Mode; No Call in Progress)			
AT+CFUN=1		15.0mA	Module full functionality with power saving disabled
AT+CFUN=4		14.0mA	Tx and Rx disabled; module is not registered on the network (Flight mode)
Multi Variant			
DRX AT+CFUN=5	GSM	2.6mA	DRx2
		2.1mA	DRx5
	WCDMA	2.1mA	DRx7
		1.9mA	DRx8
	LTE	2.4mA	Paging cycle #128 frames (1.28 sec DRx cycle)

Mode		Average(Typ.)	Mode Description
	LTE	2.1mA	Paging cycle #256 frames (2.56 sec DRx cycle)
Single Variant / ThreaddX			
DRX	LTE	2.1mA	Paging cycle #128 frames (1.28 sec DRx cycle)
AT+CFUN=5		1.8mA	Paging cycle #256 frames (2.56 sec DRx cycle)
Operative Mode(LTE)			
LTE(max power)		860mA	LTE CAT 1/CAT 4 channel BW 10 MHz, RB=12, Tx = Max power
		890mA	LTE CAT 1/CAT 4 channel BW 20 MHz, RB=Full RB, Tx = Max power With FTP TpT session LTE to USB 10Mbps DL/5Mbps UL (CAT 1) 150Mbps DL/50Mbps UL (CAT 4)
LTE(0dBm)		270mA	LTE CAT 1/CAT 4 channel BW 10 MHz, RB=12, Tx = 0 dBm
		300mA	LTE CAT 1/CAT 4 channel BW 20 MHz, RB=Full RB, Tx = 0 dBm With FTP TpT session LTE to USB 10Mbps DL/5Mbps UL (CAT 1) 150Mbps DL/50Mbps UL (CAT 4)
Operative Mode(WCDMA)			
WCDMA Voice		330mA	WCDMA voice call (Tx = 10 dBm)
WCDMA HSDPA (0 dBm)		220mA	WCDMA data call (Cat 14, Tx = 0 dBm, Max throughput)
WCDMA HSDPA (22 dBm)		640mA	WCDMA data call (Cat 14, Tx = 22 dBm, Max throughput
Operative Mode (GSM)			
GSM Tx and Rx mode			
GSM900 PL5		330mA	GSM voice call
DCS1800 PL0		220mA	
GPRS 2 Tx + 1 Rx			
GSM 900 PL5		510mA	GPRS Sending Data mode (CS-4)
DCS 1800 PL0		340mA	
Operative Mode (GPS/GNSS)			
GPS/GNSS tracking		40mA	LTE connection is idle
PSM Mode			
AT+CPSMS=1		10uA	No current source or sink by any connected pin

* Worst/best case current values depend on the network configuration, not under module control.

Note: The electrical design for the power supply must ensure a peak current output of at least 2.4A.

Note: In GSM/GPRS mode, the RF transmission is not continuous, but is packed into bursts at a base frequency of approximately 216 Hz with relative current peaks up to about 2.0A. Therefore, the power supply must be designed to withstand these current peaks without large voltage drops. This means that both the electrical design and the board layout must be designed for this current flow.If the PCB layout is not well designed, a strong noise floor is generated on the ground. This will be reflected on all audio paths producing an annoying audible noise at 216 Hz.If the voltage drops during the peaks, the current absorption is too high. The device may even shut down as a consequence of the supply voltage drop.

Table provides typical current consumption values of WE866C6-P for the various available modes.

Typical Power Consumption for WLAN Low-Power States		
Mode	Total power consumption [mA]	Mode Description
Standby	0.2	Deep Sleep
Power Save,2.4GHz	1.3	DTIM=1
	0.8	DTIM=3
	0.6	DTIM=10
Power Save,5GHz	1.5	DTIM=1
	0.8	DTIM=3
	0.7	DTIM=10

Typical Power Consumption for WLAN Continuous Rx [2.4 GHz]	
Rate	Total power consumption [mA]
11b 1Mbps	60
11b 11Mbps	62
11g 54Mbps	70
MCS0 HT20	67
MCS7 HT20	69

Typical Power Consumption for WLAN Continuous Rx [5 GHz]	
Rate	Total power consumption [mA]
MCS0 HT20	96
MCS7 HT20	94
MCS8 VHT20	112
MCS0 HT40	94
MCS7 HT40	99
MCS8 VHT40	115
MCS9 VHT40	100
MCS7 VHT80	130
MCS8 VHT80	162
MCS9 VHT80	131

Typical Power Consumption for WLAN Continuous Tx [2.4 GHz]	
Rate	Total power consumption [mA]
11b 1Mbps	365
11b 11Mbps	362
11g 54Mbps	340
MCS0 HT20	348
MCS7 HT20	335

Typical Power Consumption for WLAN Continuous Tx [5 GHz]	
Rate	Total power consumption [mA]
MCS0 HT20	495
MCS7 HT20	432
MCS8 VHT20	422
MCS0 HT40	475
MCS7 HT40	435
MCS8 VHT40	432
MCS9 VHT40	429
MCS7 VHT80	440
MCS8 VHT80	438
MCS9 VHT80	436

Typical Power consumption for BT	
Rate	Total power consumption [mA]
Continuous Rx burst	25
Continuous TX Class 2 (+4 dBm)	42
1.28 sec page scan (non-interlaced)	0.36
1.28 sec LE ADV	0.23
1.28 sec Sniff as master	0.21
1.28 sec Sniff as slave	0.26

Note: Current consumptions specification refers to typical samples and typical material. Values represent an average measurement done over few seconds. Values may vary depending on network and environmental conditions.

2.3. Electrical Design Guidelines

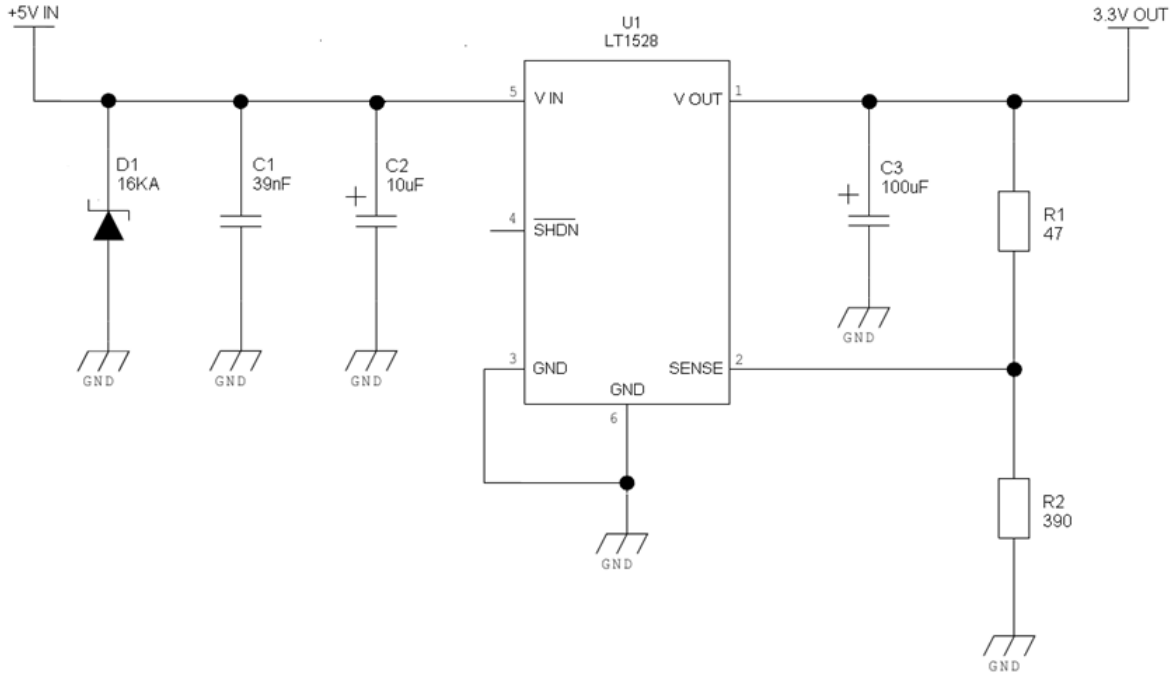
The electrical design of the power supply strongly depends on the power source where this power is drained.

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)

2.2.1 +5V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.3V, so there's not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suitable because of the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided in order to dissipate the generated heat.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the Module, a 100µF capacitor is usually suitable.
- Make sure the low ESR capacitor on the power supply output rated at least 10V.

An example of linear regulator with 5V input is:



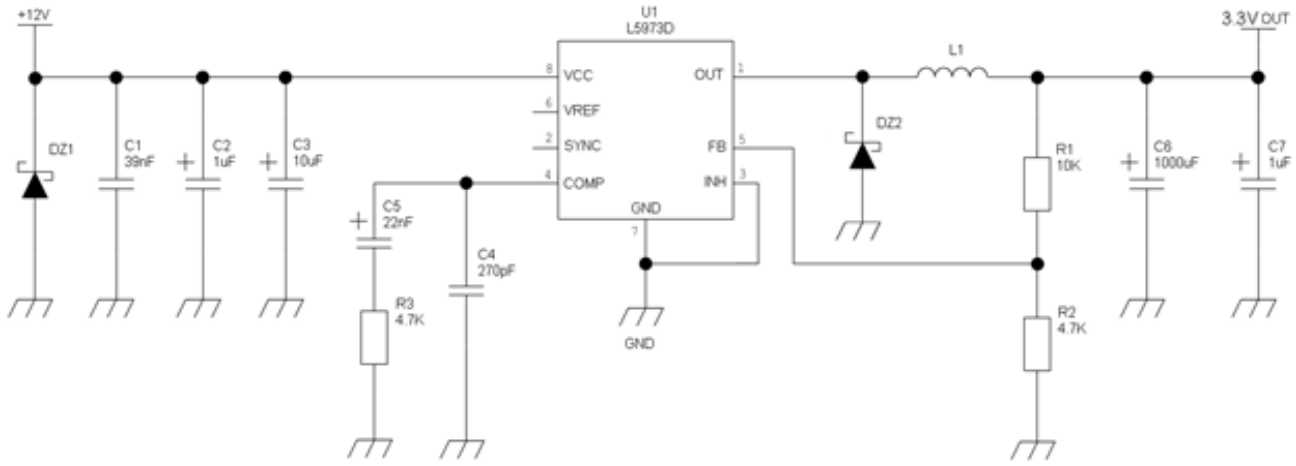
2.2.2 +12V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.3V, so due to the big difference between the input source and the desired output, a linear regulator is not suitable and shall not be used. A switching power supply will be preferable because of its better efficiency.
- When using a switching regulator, a 500kHz or more switching frequency regulator is

preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.

- In any case the frequency and Switching design selection is related to the application to be developed since the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15.8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF capacitor is usually suitable.
- Make sure the low ESR capacitor on the power supply output is rated at least 10V.
- For Car applications, a spike protection diode should be inserted close to the power input, in order to clean the supply from the spikes.

An example of switching regulator with 12V input is in the below schematic:



2.4. Thermal Design Guidelines

The thermal design of the application board and the power supply heat sink should be done with the following specifications:

- Typical average current consumption during RYW9000_Series Mini PCIe transmission @ Max PWR level at min battery level (LTE) : 700 mA
- Average current during idle (USB enabled): 30 mA
- Average current during idle (USB disabled): 5 mA
- Average current during airplane mode (USB disabled): 2 mA

Considering the very low current during Idle, especially if the Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs significant current mainly during the Data session. In LTE/WCDMA/HSPA mode, the RYW9000_Series Mini PCIe emits RF signals continuously during transmission. Therefore, special attention must be pain to how to dissipate the heat generated.

2.5. Power Supply PCB Layout Guidelines

The GSM system is made in a way that the RF transmission is not continuous, otherwise it is packed into bursts at a base frequency of about 216 Hz, and the relative current peaks can be as high as about 2.4A. Therefore the power supply must be designed in such a way to withstand with these current peaks without large voltage drops; this means that both the electrical design and the board layout must be designed for this current flow. If the voltage drop during the peak current absorption is too much, then the device may even shutdown as a consequence of the drop in the supply voltage.

Note: The electrical design for the Power supply should be made ensuring it will be capable of a peak current output of at least 2.4 A.

As seen on the electrical design guidelines, the power supply shall have a low ESR capacitor on the output to cut the current peaks on the input to protect the supply from spikes. The placement of this component is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the performance of the power supply.

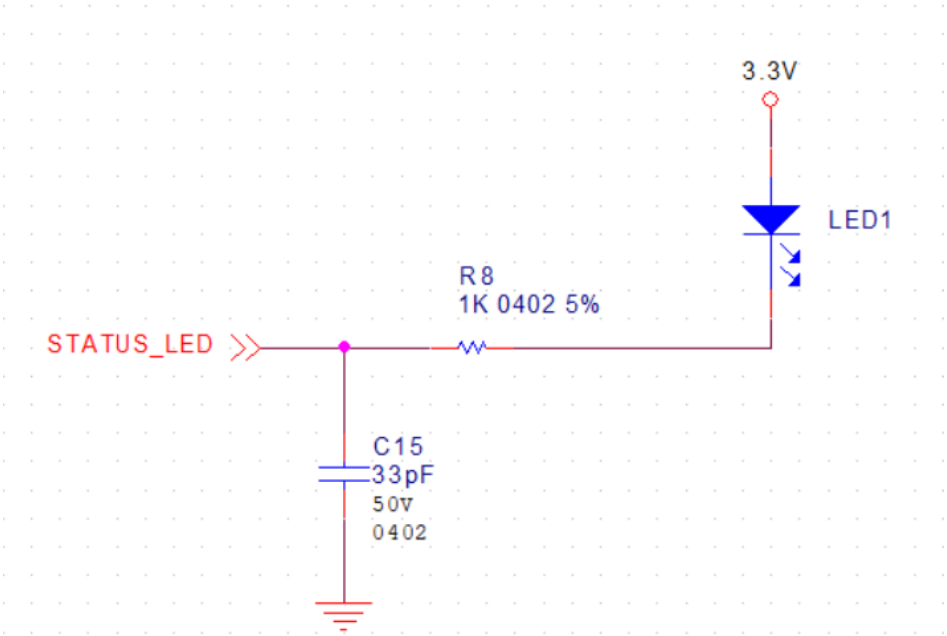
- The Bypass low ESR capacitor must be placed close to the RYW9000_Series -mPCIe power input pads or if the power supply is of the switching type it can be placed near the inductor to cut the ripple provided the PCB trace from the capacitor to the RYW9000_Series -mPCIe is wide enough to ensure a dropless connection even during an 1A current peak.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when a 1A current peak is absorbed.
- The PCB traces to the RYW9000_Series -mPCIe and the Bypass capacitor must be wide enough to ensure that no significant voltage drops occur. This is for the same reason as previous point. Try to keep this trace as short as possible.
- To reduce the EMI due to switching, it is important to keep the mesh involved very small; therefore the input capacitor, the output diode (if not embodied in the IC) and the regulator have to form a very small loop. This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).
- A dedicated ground for the Switching regulator separated by the common ground plane is suggested.
- The placement of the power supply on the board should be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables should be kept separate from noise sensitive lines such as microphone/earphone cables.
- The insertion of EMI filter on VBATT pins is suggested in those designs where antenna is placed close to battery or supply lines.

- A ferrite bead like Murata BLM18EG101TN1 or Taiyo Yuden P/N FBMH1608HM101 can be used for this purpose.

3. DIGITAL SECTION

3.1. STATUS_LED

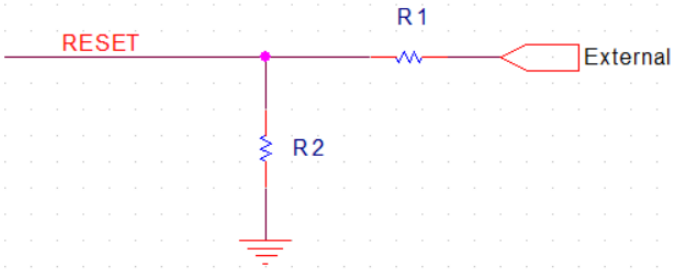
STATUS_LED is driven, by default, by the module according the PCI Express Mini Card Electromechanical Specification Revision 2.1. If desired, LED behavior can be configured by adjusting the software settings. The following picture shows the internal STATUS_LED driver and the recommended connection to a LED:



Note: THIS SIGNAL IS NOT ACTIVE BY DEFAULT. REFER TO AT#SLED DESCRIPTION IN THE AT COMMAND USER GUIDE.

3.2. RESET

To unconditionally shut down the RYW9000_Series -mPCIe module, the RESET pad must be tied low for at least 1000 milliseconds and then released.
Figure shows a simple circuit for applying an unconditional shutdown.



Note: Recommended values are as follows: R2 = 47kΩ, R1 = 10kΩ.

Note: Do not use any pull-up resistor on the RESET line or any totem pole digital output. Using a pull-up resistor may cause latch-up problems on the RYW9000_Series -mPCIe power regulator and improper functioning of the module. The RESET line must be connected only in an open-collector configuration.

Note: The Unconditional Hardware Shutdown must always be implemented on the boards, but this function must use it only as an emergency exit procedure, and not as a normal power-off operation.
Use the AT#SHDN command instead.

3.3. USB Port

The RYW9000_Series -mPCIe module includes a Universal Serial Bus (USB) transceiver, which operates at USB high-speed (480 Mbits/sec). It can also operate with USB full-speed hosts (12 Mbits/sec).

It is compliant with the USB 2.0 specification and can be used for control and data transfers as well as for diagnostic monitoring and firmware update.

The USB port is typically the main interface between the RYW9000_Series -mPCIe module and OEM hardware.

Note: The USB_D+ and USB_D- signals have a clock rate of 480 MHz. The signal traces must be routed carefully. Minimize trace lengths, number of vias, and capacitive loading. The impedance value should be as close as possible to 90 Ohms differential.

Table below lists the USB interface signals:

Signal	Pin	Usage
USB_D-	36	Minus (-) line of the differential, bi-directional USB signal to/from the peripheral device
USB_D+	38	Plus (+) line of the differential, bi-directional USB signal to/from the peripheral device

3.4. Serial Port

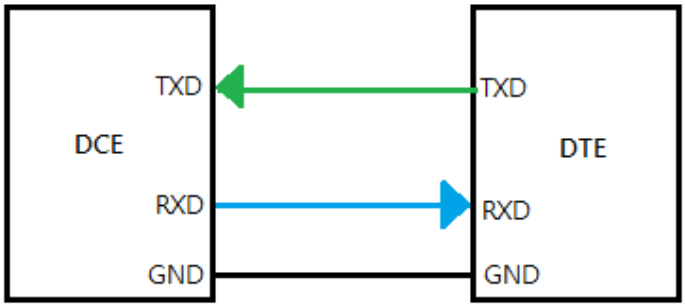
The serial port is typically a secondary interface between the RYW9000_Series -mPCIe module and OEM hardware. MODEM SERIAL PORT is available on RYW9000_Series -mPCIe adaptor

Several configurations can be designed for the serial port on the OEM hardware.
The most common configurations are:

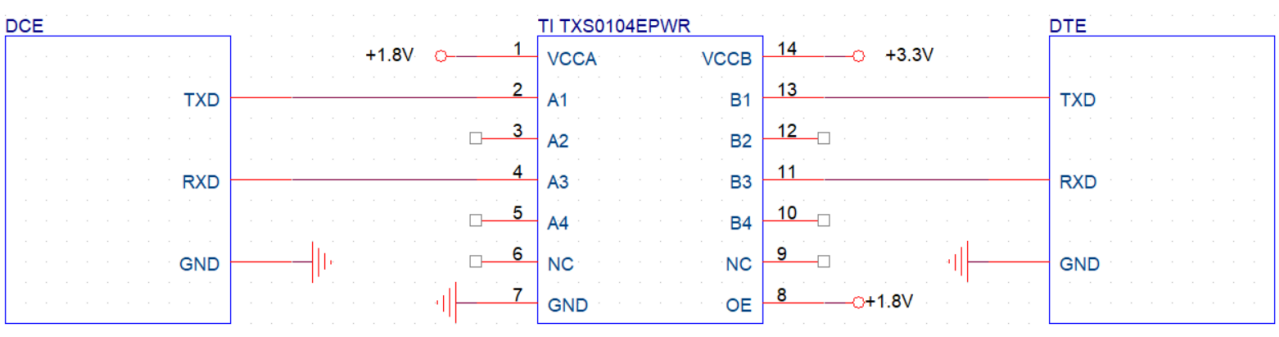
- RS232 PC com port
- Microcontroller UART @ 1.8V (Universal Asynchronous Receive Transmit)
- Microcontroller UART @ 3.3V/5V or other voltages different from 1.8V

Depending on the type of serial port on the OEM hardware, a level translator circuit may be needed to make the system operate. The only configuration that does not need level translation is the 1.8V UART.

Microcontroller UART @ 1.8V application circuit:

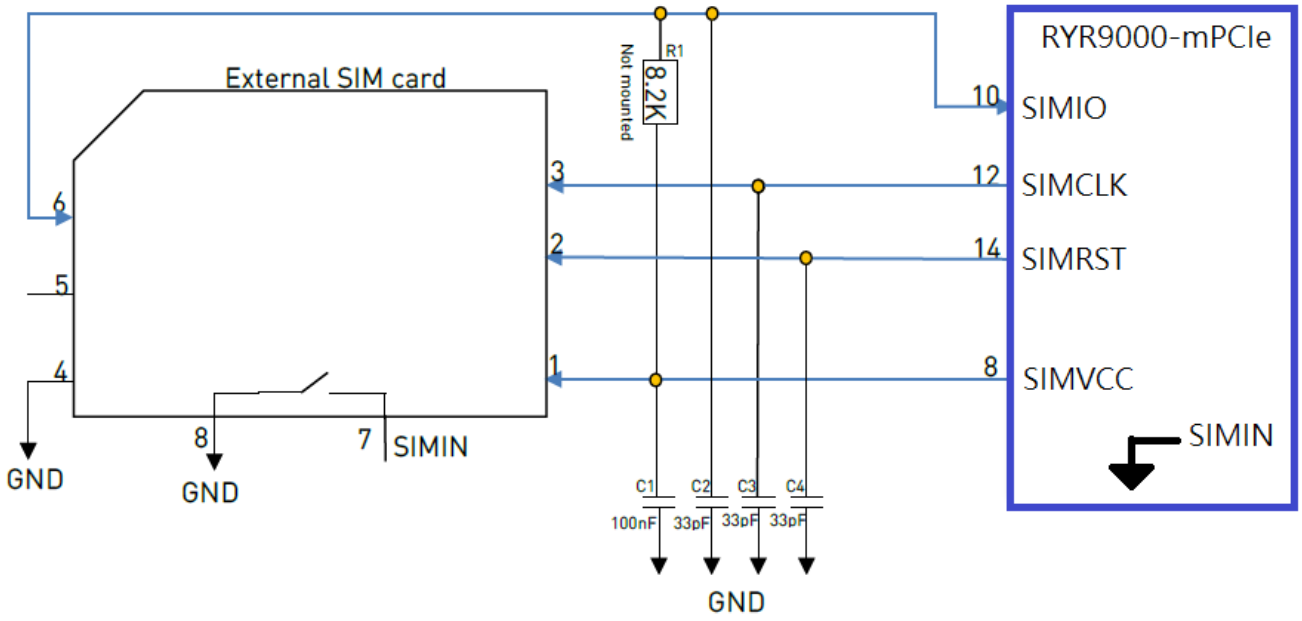


Microcontroller UART @ 3.3V/5V application circuit:



3.5. SIM Interface

The SIM pins provide the connections necessary to interface to a SIM socket located on the host device. The Voltage levels over this interface comply with 3GPP standards. SIMIN line terminated to GND internally for standard RYW9000_Series variant without either SIM holder or onboard eSIM.



Note: The resistor value on SIMIO pulled up to SIMVCC should be defined accordingly in order to be compliant with 3GPP specification. RYW9000_Series - mPCIe contains an internal pull-up resistor on SIMIO. However, the un-mounted option in the application design can be recommended in order to tune R1 if necessary.

4. RF SECTION

4.1. Band Variants

RYW9000_Series -mPCIe modules bands combinations are listed below:

Ordering	2G Band	HSPA+	LTE FDD	LTE TDD	TD-SCDMA
RYW94AP	-	1,5,6,8,19	1, 3, 5, 8, 9, 18, 19, 26, 28	-	-
RYW94EU	3,8	1,3,8	1,3,7,8,20,28A	-	-
RYW94NF	-	2,4,5	2, 4, 5, 12, 13, 14, 66, 71	-	-
RYW94LA	2,3,5,8	1,2,4,5	1,2,3,4,5,7,28	-	-
RYW94CN	3,8	1,8	1,3,5,8	38,39,40,41	34,39

Parameter	Conditions	Frequency Range
WLAN Center channel frequency for 2.4 GHz	Center frequency at 5 MHz spacing	2.412 – 2.484 GHz
WLAN Center channel frequency for 5 GHz	Center frequency at 5 MHz spacing	4.9 – 5.925 GHz
BT Frequency range	BT Specification: 2.4 ≤ f ≤ 2.4835 Center frequency f = 2402 + k, where k is the channel number.	2402 – 2480 MHz

4.2. Antenna Connectors

The RYW9000_Series -mPCIe adapter is equipped with a set of 50 Ω RF U.FL. connectors from Hirose U.FL-R-SMT-1.

The available connectors are:

The presence of all the connectors depends on the product characteristics and the supported functionalities.

For more information about mating connectors, visit the website https://www.hirose.com/
The antenna connection is one of the most important aspect in the full product design as it strongly affects the product overall performances, so please read carefully and follow the requirements and the guidelines for a proper design.
The RYW9000_Series -mPCIe adapter is provided with three RF connectors.

The available connectors are:

- Main RF antenna (ANT)
- RX Diversity Antenna (DIV)
- GNSS Antenna (GPS)
- WiFi & Bluetooth

Connecting cables between the module and the antenna must have an impendance of 50 Ω.
If the module impedance does not match, the RF performance is reduced significantly.
If the host device is not designed to use the module diversity or the GPS antenna, terminate the interface with a 50Ω load.

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